CLAIMS

1   1. A circuit comprising:

2   a reference signal;

3   a frequency synthesizer, receiving a dithered signal and the reference signal,

4   generating a constant frequency output; and

5   configuration registers transceiving data and control signals with the frequency

6   synthesizer.

1   2. A circuit, as defined in claim 1, further comprising a modulated analog phase

2   lock loop, receiving the reference signal, generating the dithered signal.

1   3. A circuit, as defined in claim 1, the frequency synthesizer comprising:

2   a predictor and corrector that receive the dithered signal and the reference signal,

3   generating a "remove pulse" signal; and

4   an output generator, receiving the dithered signal, reference signal, and "remove

5   pulse" signal, generating a "clear pulse" signal and the constant frequency output.

1   4. A circuit, as defined in claim 1, the frequency synthesizer comprising:

2   a predictor, generating a first output signal indicative of the average number of

3   dithered periods to remove per dithered period;

4   a corrector receiving the first output signal, generating a second output signal

5   indicative of the fractional number of dithered periods to remove each dithered period;

6   and

7   an accumulator receiving the second output signal, operative to count the

8   fractional number of dithered periods, removing a dithered period when an integer has

9   been reached.

1   5. A circuit, as defined in claim 4, the predictor comprising:

2   means for measuring the average number of dithered periods for the sample of the

3   reference signal;

4   a comparator, receiving the first output signal and a desired number of dithereds

5 periods per sample of the reference signal, generating a difference indicative of the

6 average number of dithered periods to remove per sample of the reference signal; and

7   a multiplier, receiving the difference, operative to scale the difference according

8 to a scale factor register value.

1   6. A circuit, as defined in claim 4, the corrector comprising:

2   means for measuring error from the last sample;

3   means for determining a scale to fractional error; and

4   an adder, receiving the scale to fractional error and the average number of

5 dithered periods to remove per dithered period, generating the difference.

1   7. A circuit, as defined in claim 1, the frequency synthesizer including:

2   a first synchronizer, receiving the system clock as reference input and the PLL

3 output, generating a first output;

4   an edge detector, receiving the first output and the PLL output, generating an edge

5 signal;

6   a second synchronizer, receives an enable signal and the system clock, generating

7 a second output;

8   an adder, receiving reference count signals, generating adder output signals;

9   an Expected Count Latch, receiving the second output as a clear input, the system

10 clock as a clock input, the adder output signals as data, and the edge signal as a load

11 signal, generating a latch output;

12   wherein the adder further receives the latch output;

13   an Edge Counter, receiving the system clock and the second output as a clear

14 signal, generating a counter output;

15   a comparator, receiving the counter output and the latch output, generating a

16 rollover output, an A>B+1 signal, and an A>B signal.

1   8. A method for frequency synthesis comprising:

2   receiving a dithered signal and a reference signal;

3   selecting a desired number of periods in the dithered signal to receive during a

4   sample period of the reference signal;

5   counting the actual number of periods in the dithered signal during the sample

6   period;

7   comparing the desired number to the actual number;

8   generating a constant frequency signal based on the comparison.

1   9. A method for frequency synthesis comprising:

2   receiving a dithered signal and a reference signal;

3   determining an average fractional number of dithered periods of the dithered

4   signal to remove each dithered period;

5   determining a fractional error of dithered periods for each dithered period based

6   on a period of the reference signal; and

7   combining the average fractional number and the fractional error generating a

8   fractional number of dithered periods to remove each dithered period; and

9   generating a constant frequency signal based on the combination.

1   10. A method for frequency synthesis, as claimed in 9, determining an average

2   fractional number of dithered periods comprising:

3   measuring an average number of dithered periods for a sample of the reference

4   signal;

5   generating a difference from the average number of dithered periods and a desired

6   number of dithered periods per sample of the reference signal, the difference indicative of

7   the average number of dithered periods to remove per sample of the reference signal; and

8   scaling the difference according to a scale factor register value.

1   11. A method for frequency synthesis, as defined in claim 9, determining a

2   fractional error of dithered periods for each dithered period comprising:

3   measuring error in a number of dithered periods corresponding to a given sample

4   of the reference signal;

5   determining a scale to fractional error; and

6   scaling the scale to fractional error to generate the fractional error.

1   12. A method for frequency synthesis, as defined in claim 11, wherein

2   determining a scale to fractional error comprises referring to a look-up table.

1   13. An apparatus for frequency synthesis comprising:

2   a predictor operative to estimate an average amount of correction per sample;

3   a corrector operative to measure actual error in a previous sample;

4   an accumulator, connected to the predictor and corrector, generating an

5   accumulator output signal indicative of the sum of the average amount of correction and

6   the actural error;

7   an output generator, receiving the accumulator output signal, generating an output

8   signal having constant frequency.